

PAPI - PERFORMANCE API

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- Application and functions execution time is easy to measure
 - * time
 - * gprof
 - * valgrind (callgrind)
 - *

- Application and functions execution time is easy to measure
 - * time
 - * gprof
 - * valgrind (callgrind)
 - *
- * It is enough to identify bottlenecks, but...
 - * Why is is it slow?
 - * How does the code behaves?

* Efficient algorithms should take into account

Cache behaviour

- Cache behaviour
- Memory and resource contention

- Cache behaviour
- Memory and resource contention
- * Floating point efficiency

- Cache behaviour
- Memory and resource contention
- * Floating point efficiency
- Branch behaviour

HW Performance Counters

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 Hardware designers added specialised registers o measure various aspects of a microprocessor

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- Hardware designers added specialised registers o measure various aspects of a microprocessor
- * Generally, they provide an insight into
 - Timings
 - Cache and branch behaviour
 - Memory access patterns
 - Pipeline behaviour
 - * FP performance
 - * IPC
 - *

What is PAPI?

What is PAPI?

Interface to interact with performance counters

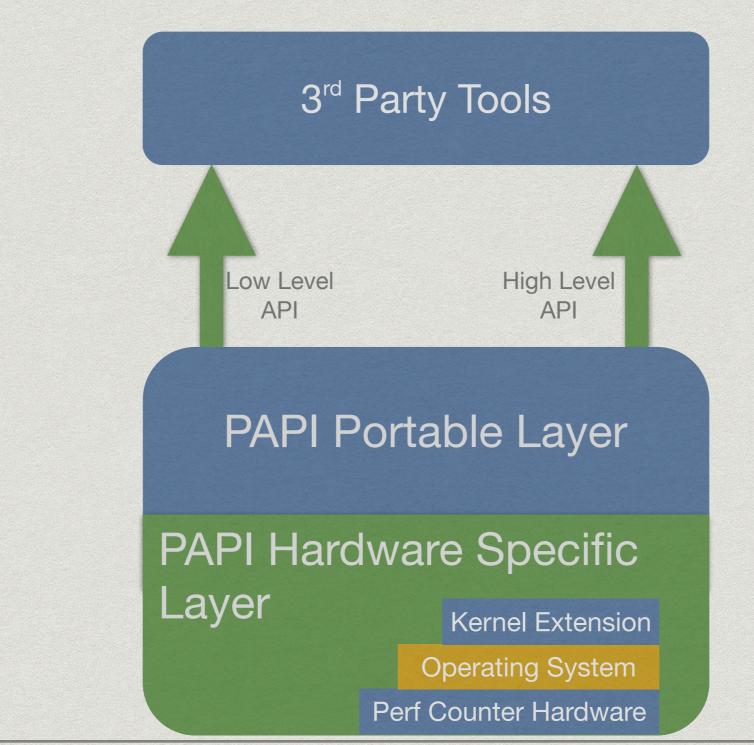
- With minimal overhead
- Portable across several platforms

What is PAPI?

Interface to interact with performance counters

- With minimal overhead
- Portable across several platforms
- * Provides utility tools, C, and Fortran API
 - Platform and counters information

PAPI Organisation



André Pereira, UMinho, 2018/2019

Supported Platforms

Mainstream platforms (Linux)

- * x86, x86_64 Intel and AMD
- * ARM, MIPS
- Intel Itanium II
- * IBM PowerPC

Utilities

Utilities

* papi_avail

	1. am	pereira	l@com	pute-552-2:~/tools/papi-gcc4.9.0/bin (ssh)					
PAPI Version		: 5.3.2.0							
Vendor string and code									
Model string and code		: Intel(R) Xeon(R) CPU E5-2670 v2 @ 2.50GHz (62)							
CPU Revision		: 4.000000							
CPUID Info		: Family: 6 Model: 62 Stepping: 4							
CPU Max Megahertz		: 250	1						
CPU Min Megahertz		: 120	0						
Hdw Threads per core		: 2							
		: 10							
Sockets		: 2							
NUMA Nodes		: 2							
CPUs per Node		: 20							
Total CPUs		: 40							
Running in a VM		: no							
Number Hardwa	are Counters	: 11							
Max Multiple	<pre>K Counters</pre>	: 32							
Name	Code /	Avail	Deriv	Description (Note)					
PAPI_L1_DCM	0x80000000	Yes	No	Level 1 data cache misses					
PAPI_L1_ICM	0x80000001	Yes	No	Level 1 instruction cache misses					
PAPI_L2_DCM	0x80000002	Yes	Yes	Level 2 data cache misses					
PAPI_L2_ICM		Yes	No	Level 2 instruction cache misses					
PAPI_L3_DCM	0x80000004	No	No	Level 3 data cache misses					
PAPI_L3_ICM		No	No	Level 3 instruction cache misses					
PAPI_L1_TCM	0x80000006	Yes	Yes	Level 1 cache misses					
PAPI_L2_TCM		Yes	No	Level 2 cache misses					
PAPI_L3_TCM		Yes	No	Level 3 cache misses					
PAPI_CA_SNP		No	No	Requests for a snoop					
PAPI_CA_SHR		No	No	Requests for exclusive access to shared cache line					
PAPI_CA_CLN		No	No	Requests for exclusive access to clean cache line					
PAPI_CA_INV		No	No	Requests for cache line invalidation					
PAPI_CA_ITV		No	No	Requests for cache line intervention					
PAPI_L3_LDM		No	No	Level 3 load misses					
PAPI_L3_STM		No	No	Level 3 store misses					
PAPI_BRU_IDL		No	No	Cycles branch units are idle					
PAPI_FXU_IDL		No	No	Cycles integer units are idle					
PAPI_FPU_IDL		No	No	Cycles floating point units are idle					
PAPI_LSU_IDL		No	No	Cycles load/store units are idle					
PAPI_LS0_IDL PAPI_TLB_DM		Yes	Yes	Data translation lookaside buffer misses					
PAPI_TLB_IM	0x80000015	Yes	No	Instruction translation lookaside buffer misses					
PAPI_TLB_TM PAPI_TLB_TL	0x80000015 0x80000016	No	No	Total translation lookaside buffer misses					
PAPI_TLB_TL PAPI_L1_LDM	0x80000010 0x80000017	Yes	No	Level 1 load misses					
PAPI_LI_LDM PAPI_L1_STM	0x80000017 0x80000018	Yes	No	Level 1 store misses					
PAPI_LI_SIM PAPI_L2_LDM	0x80000018 0x80000019	No	No	Level 2 load misses					
PAPI_L2_LDM PAPI_L2_STM	0x80000019 0x8000001a	Yes	NO	Level 2 toda misses Level 2 store misses					
PAPI_LZ_SIM PAPI_BTAC_M	0x8000001d 0x8000001b	No	NO NO	Branch target address cache misses					
PAPI_BTAC_M PAPI_PRF_DM				Data prefetch cache misses					
PAPI_PKF_DM	0x8000001c	No	No	buta prefetch cache misses					

Utilities

* papi_avail

* papi_native_avail

	1. ampereira@compute-552-2:~/tools/papi-gcc4.9.0/bin (ssh)	
1	monitor at kernel level	
TLB_ACCESS	;	
1	TLB access	
I :STLB_	HIT	
1	Number of load operations that missed L1TLB but hit L2TLB	
I :LOAD_	STLB_HIT	
	Number of load operations that missed L1TLB but hit L2TLB	
l :e=0		
	edge level (may require counter-mask >= 1)	
:i=0	invert	
l :c=0	Livert	
I .C=0	counter-mask in range [0-255]	
' :t=0		
I .c=0	measure any thread	
l :u=0		
I	monitor at user level	
l :k=0		
I	monitor at kernel level	
		-
I TLB_FLUSH		
	TLB flushes	
I :DILB_	THREAD	
I:STLB_	Number of DTLB flushes of thread-specific entries	
I .31LB_	Number of STLB flushes	
:e=0		
l	edge level (may require counter-mask >= 1)	
i=0		
I	invert	
l :c=0		
I	counter-mask in range [0-255]	
l :t=0		
	measure any thread	
l :u=0		
l :k=0	monitor at user level	
I :K=0	monitor at kernel level	
۱ 		
I UNHALTED_(ORE CYCLES	
	Count core clock cycles whenever the clock signal on the specific	
I	core is running (not halted)	
l :e=0		
1	edge level (may require counter-mask >= 1)	
l :i=0		
1	invert	
l :c=0		
	counter-mask in range [0-255]	

André Pereira, UMinho, 2017/2018

Utilities

* papi_avail

- * papi_native_avail
- * papi_event_chooser

1. ampereira@compute-552-2:-/tools/papi-gcc4.9.0/bin (ssh) Compereira@compute-552-2 bin]3 ./papi_event_chooser PRESET PAPI_PQPS Event Chooser: Available events which can be added with given events. PAPI Version : 5.3.2.0 Vendor string and code : GenuineIntel (1) Model string and code : GenuineIntel (1) Model string and code : Family: 6 Model: 62 Stepping: 4 (PUI Max Megahertz : 2501 (PU Min Megahertz : 2501 (PU Min Megahertz : 120 Hdw Threads per core : 2 Cores per Socket : 10 Sockets : 2 NUMA Nodes : 2 Cores per Socket : 10 Number Hardware Counters : 11 Max Multiplex Counters : 32 Number Nadware Counters : 32 Number Nadware Counters : 32 Number Nadware Counters : 32 Number Nadware Counters : 32 Name Code Deriv Description (Note) PAPI_LLI_DOM 0x800000007 No Level 1 instruction cache misses PAPI_LI_TIM 0x8000007 No Level 2 cache misses PAPI_LI_TIM 0x8000007 No Level 2 cache misses PAPI_LI_TIM 0x8000007 No Level 2 cache misses PAPI_LI_TIM 0x8000007 No Level 1 store misses PAPI_LI_TIM 0x8000007 No Level 2 store misses PAPI_LI_TIM 0x8000007 No Level 1 load misses PAPI_LI_TIM 0x80000007 No Level 1 conter misses PAPI_LI_TIM 0x8000007 No Level 1 conter misses PAPI_LI_TIM 0x8000007 No Level 1 store misses PAPI_LI_TIM 0x8000007 No Level 2 store misses PAPI_LI_TIM 0x8000007 No Level 1 load misses PAPI_LI_TIM 0x8000007 No Level 1 store misses PAPI_LI_TIM 0x8000007 No Level 1 load misses PAPI_LI_TIM 0x8000007 No Level 2 store misses PAPI_LI_TIM 0x8000007 No Level 1 store misses PAPI_LI_TIM 0x8000007 No Level 1 store misses PAPI_LI_TIM 0x8000007 No Level 1 load misses PAPI_LI_TIM 0x8000007 No Level 1 store misses PAPI_LI_TIM 0x8000007 No Level 1 load misses PAPI_LI_TIM 0x8000007 No Level 1 store misses PAPI_LI_TIM 0x8000007 No Level 2 store misses PAPI_LI_TIM 0x8000007 No Level 1 load misses PAPI_LI_TIM 0x8000007 No Level 2 store misses						
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André Pereira, UMinho, 2018/2019

* Preset events

- Events implemented on all platforms
 - * PAPI_TOT_INS

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- Events implemented on all platforms
 - * PAPI_TOT_INS
- * Native events
 - * Platform dependent events
 - * L3_CACHE_MISS
- * Derived events
 - * Preset events that are derived from multiple native events
 - * PAPI_L1_TCM may be L1 data misses + L1 instruction misses

* Calls the low-level API

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- * Easier to use

André Pereira, UMinho, 2018/2019

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 - You will not optimise code based on the amount of L2
 TLB flushes per thread...

- * Calls the low-level API
- * Easier to use
- * Enough for coarse grain measurements
 - You will not optimise code based on the amount of L2
 TLB flushes per thread...
- * For preset events only!

The Basics

- * PAPI_start_counters
- * PAPI_stop_counters

The Basics

```
#include "papi.h"
#define NUM_EVENTS 2
long long values[NUM_EVENTS];
unsigned int Events[NUM_EVENTS]={PAPI_TOT_INS,PAPI_TOT_CYC};
/* Start the counters */
PAPI_start_counters((int*)Events,NUM_EVENTS);
/* What we are monitoring... */
do_work();
/* Stop counters and store results in values */
```

```
retval = PAPI_stop_counters(values,NUM_EVENTS);
```

PAPI Low-level Interface

PAPI Low-level Interface

Increased efficiency and functionality

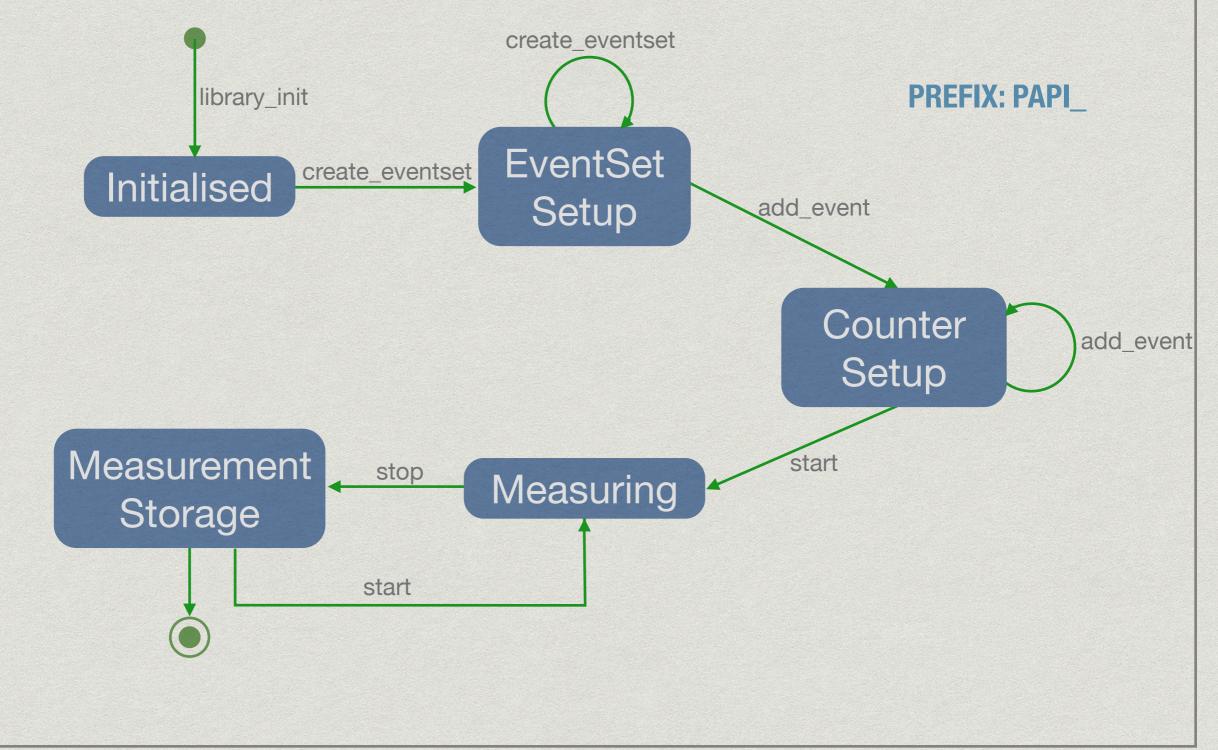
PAPI Low-level Interface

- Increased efficiency and functionality
- More information about the environment

PAPI Low-level Interface

- Increased efficiency and functionality
- More information about the environment
- * Concepts to check later
 - * EventSet
 - * Multiplexing





The Basics

#include "papi.h" #define NUM_EVENTS 2 int Events[NUM_EVENTS]={PAPI_FP_INS,PAPI_TOT_CYC}; int EventSet; long long values[NUM_EVENTS]; /* Initialize the Library */ retval = **PAPI_library_init**(**PAPI_VER_CURRENT**); /* Allocate space for the new eventset and do setup */ retval = PAPI_create_eventset(&EventSet); /* Add Flops and total cycles to the eventset */ retval = PAPI_add_events(EventSet,Events,NUM_EVENTS); /* Start the counters */ retval = PAPI_start(EventSet); /* What we want to monitor*/ do_work(); /*Stop counters and store results in values */ retval = PAPI_stop(EventSet, values);

* PAPI is also available for CUDA GPUs

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* Uses the CUPTI

- Which counters can be directly accessed
- * Define a file with the counters and an environment variable

* PAPI is also available for CUDA GPUs

* Uses the CUPTI

- Which counters can be directly accessed
- * Define a file with the counters and an environment variable
- * Gives useful information about the GPU usage
 - * IPC
 - Memory load/stores/throughput
 - Branch divergences
 - SM(X) occupancy

*

* The whole application?

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- * PAPI usefulness is limited when used alone

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 - Combine it with other profilers

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- * PAPI usefulness is limited when used alone
 - Combine it with other profilers
 - Bottleneck identification + characterisation

A Practical Example

for (int i = 0; i < SIZE; i++) for (int j = 0; j < SIZE; j++) for (int k = 0; k < SIZE; k++) c[i][j] += a[i][k] * b[k][j];

A Practical Example

int sum;

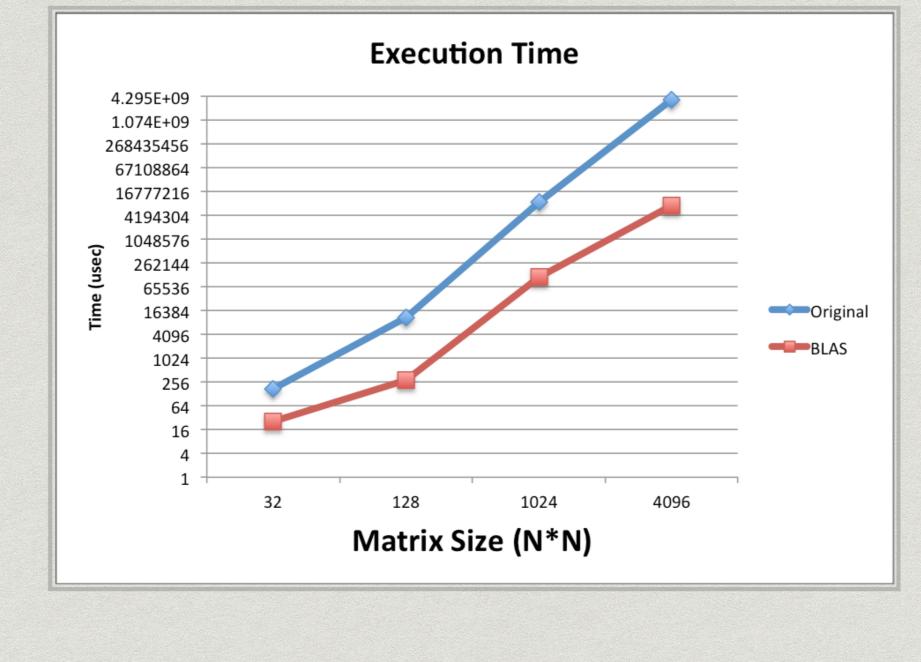
```
for (int i = 0; i < SIZE; i++)
for (int j = 0; j < SIZE; j++) {
    sum = 0;
    for (int k = 0; k < SIZE; k++)
        sum += a[i][k] * b[k][j];
    c[i][j] = sum;
}</pre>
```

A Practical Example SGEMM

int sum;

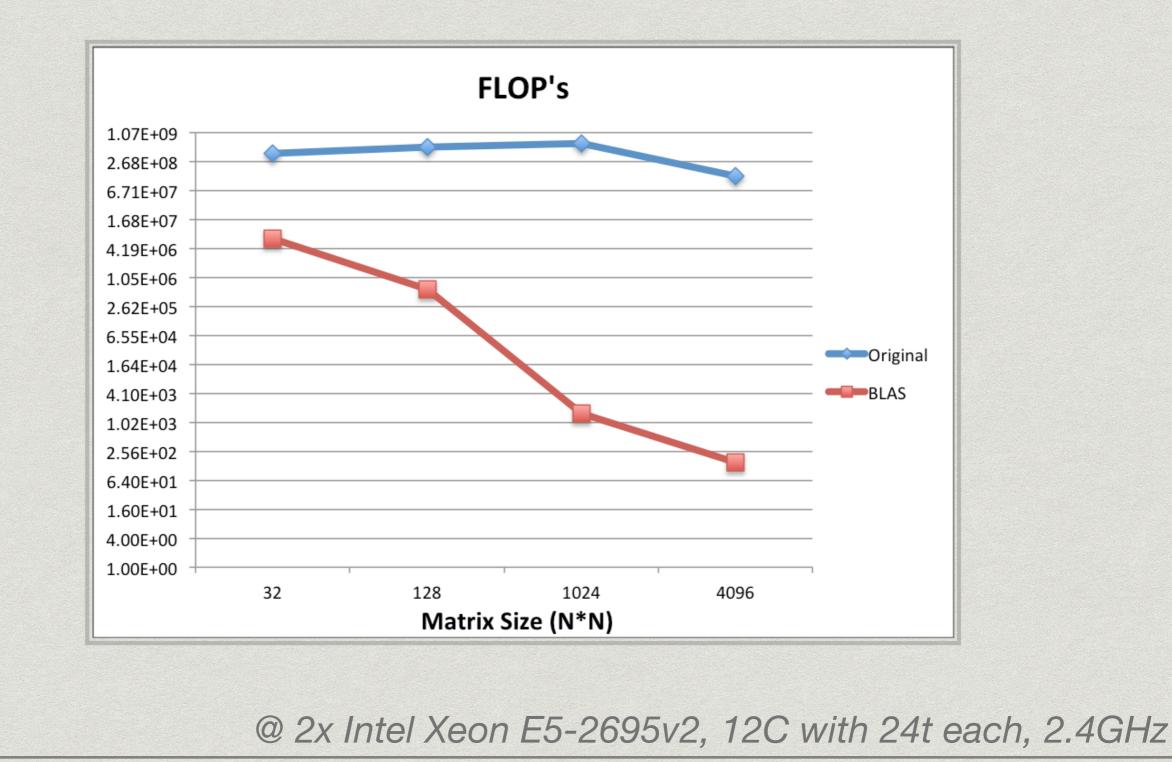
```
for (int i = 0; i < SIZE; i++)
for (int j = 0; j < SIZE; j++) {
    sum = 0;
    for (int k = 0; k < SIZE; k++)
        sum += a[i][k] * b[k][j];
    c[i][j] = sum;
}</pre>
```

Execution Time

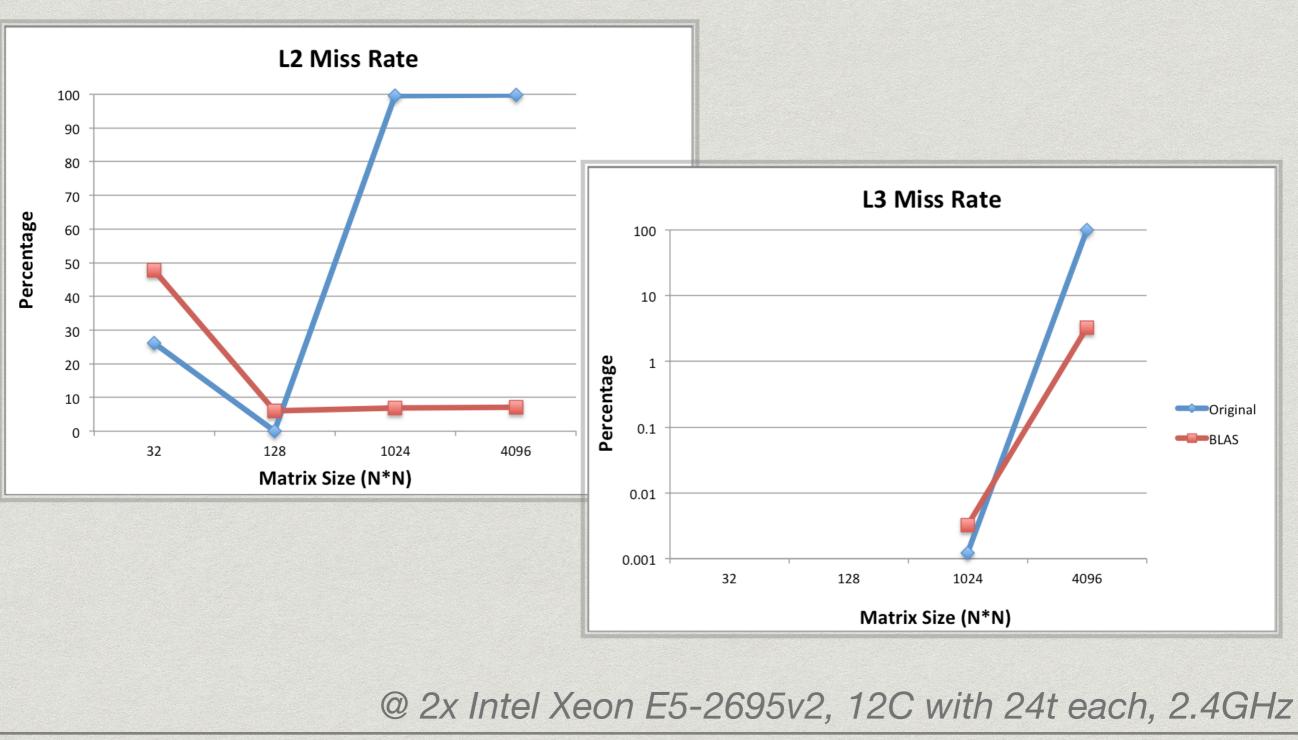


@ 2x Intel Xeon E5-2695v2, 12C with 24t each, 2.4GHz

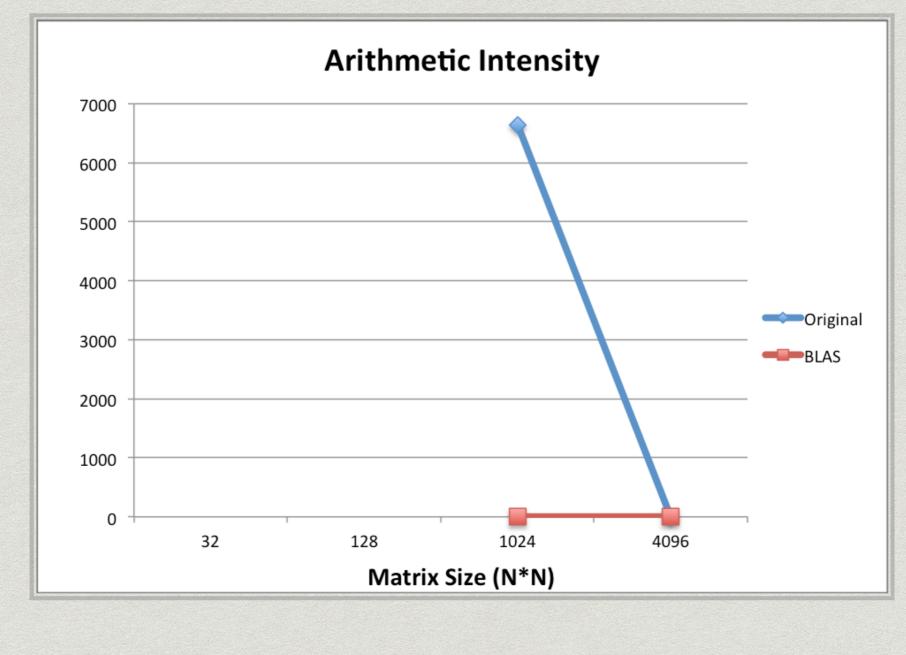
FLOP's



Cache Miss Rate

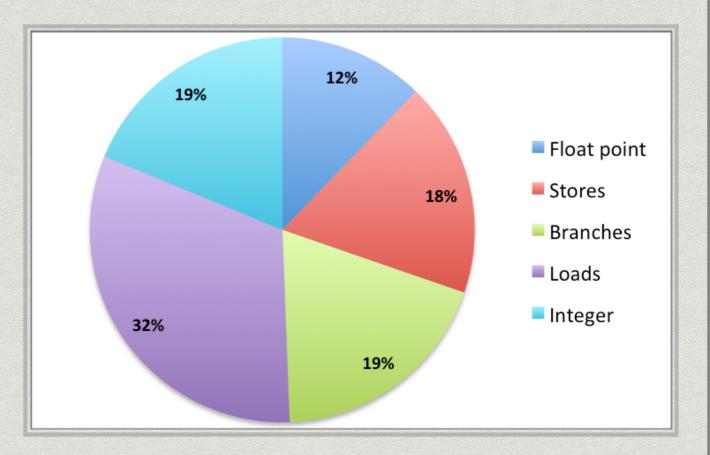


Arithmetic Intensity



@ 2x Intel Xeon E5-2695v2, 12C with 24t each, 2.4GHz

- Instruction mix
 - * PAPI_FP_INS
 - * PAPI_SR/LD_INS
 - * PAPI_BR_INS
 - * PAPI_SP/DP_VEC



- Instruction mix
 - * PAPI_FP_INS
 - * PAPI_SR/LD_INS
 - * PAPI_BR_INS
 - * PAPI_SP/DP_VEC
- * FLOPS and operational intensity
 - * PAPI_FP_OPS
 - * PAPI_SP/DP_OPS
 - * PAPI_TOT_INS

- Instruction mix
 - * PAPI_FP_INS
 - * PAPI_SR/LD_INS
 - * PAPI_BR_INS
 - * PAPI_SP/DP_VEC
- * FLOPS and operational intensity
 - * PAPI_FP_OPS
 - * PAPI_SP/DP_OPS
 - * PAPI_TOT_INS
- * Cache behaviour and bytes transferred
 - * PAPI_L1/2/3_TCM
 - * PAPI_L1_TCA

- * Be careful choosing a measurement heuristic
 - * Q: Why? Average? Median? Best measurement?

* Be careful choosing a measurement heuristic

* Q: Why? Average? Median? Best measurement?

* Automatise the measurement process

- With scripting/C++ coding
- Using 3rd party tools that resort to PAPI
 - * PerfSuite
 - * HPCToolkit
 - * TAU
 - * VTune

* Be careful choosing a measurement heuristic

* Q: Why? Average? Median? Best measurement?

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* Available for Java and on virtual machines

- * Use the same GCC/G++ version as
 - * The PAPI compilation on your home
 - * The PAPI available at the cluster

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 - The PAPI compilation on your home
 - * The PAPI available at the cluster
- Setup the environment
 - module load gcc/5.3.0
 - * module load papi/5.4.1
 - Add -I/share/apps/papi/5.4.1/include and -L/share/apps/papi/
 5.4.1/lib to the compilation if PAPI is not recognised

- * Use the same GCC/G++ version as
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 5.4.1/lib to the compilation if PAPI is not recognised
- Code compilation g++ -O3 c.cpp -lpapi

Hands-on

- Assess the available counters on a node (interactive qsub)
 - * qsub -I -qmei -Inodes=1,walltime=10:00
- Perform the FLOPs and miss rate measurements interactively
 - https://bitbucket.org/ampereira/papi/downloads

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